In the Claims

Kindly amend claims 86-87 and 100, without prejudice, and rejoin claims 206-225, as set forth below:

86. (currently amended) A method of coupling signals between electronic devices in a modular electronic system, said method comprising the steps of:

locating a first ~~co-planar~~ subset of said electronic devices **and a plurality of half-capacitors** on a first ~~planar~~ semiconductor chip;

locating a second ~~co-planar~~ subset of said electronic devices **and a plurality of half-capacitors** on a ~~planar~~ second semiconductor chip; and,

aligning and affixing said first and second chips so as to capacitively couple said first and second chips **using at least some of the half-capacitors on each of said chips**.

87. (currently amended) A method of coupling signals between electronic devices in a modular electronic system as defined in claim 86 wherein the first and second chips are affixed to a base substrate thereby capacitively coupling said first and second chips via **said** substrate.

100. (currently amended) A method of capacitively

coupling signals between first and second ~~planar~~ chips, each said chip having a plurality of ~~planar~~ half-capacitors, said method comprising the steps of:

affixing said first ~~planar~~ chip to a substrate;

aligning said second ~~planar~~ chip to said first chip; and,

affixing said second ~~planar~~ chip to said substrate, thereby capacitively coupling corresponding half-capacitors on said first and second planar chips and providing direct capacitive coupling between said first and second planar chips.

206. (previously presented) A method of fabricating an integrated circuit module, comprising:

providing a plurality of first dice, said first dice each having half-capacitors formed on a surface thereof;

providing a plurality of second dice, said second dice each having half-capacitors formed on a surface thereof; and

arranging said first dice so that each of said first dice overlaps at least three of said second dice, and each of said second dice overlaps at least three of said first

dice, thereby defining overlap areas,

wherein at least some half-capacitors of said plurality of first dice are configured to be capacitively coupled to corresponding half-capacitors of said second dice in said overlap areas.

207. (previously presented) The method of claim 206 wherein providing said plurality of first dice and second dice include forming a dielectric layer on some of said first dice and second dice, so that half-capacitors in said overlap areas are spaced apart.

208. (previously presented) The method of claim 206 wherein said plurality of first dice are rectangles.

209. (previously presented) The method of claim 206 wherein said plurality of second dice are rectangles.

210. (previously presented) The method of claim 208 wherein said plurality of second dice are squares.

211. (previously presented) The method of claim 206 wherein said plurality of first and second dice are shaped as octagons.

212. (previously presented) The method of claim 206 further comprising:

arranging said first dice to form a first two-dimensional repeating pattern; and

arranging said second dice to form a second two-dimensional repeating pattern.

213. (previously presented) The method of claim 206 further comprising:

capacitively coupling some half-capacitors of said first dice to some half-capacitors of said second dice in said overlap areas.

214. (previously presented) A method of fabricating an integrated circuit module, comprising:

providing a plurality of first dice, said first dice each having first half-capacitors formed on a surface thereof;

providing a plurality of second dice, said second dice each having second half-capacitors formed on a surface thereof; and

arranging said first dice so that each first die overlaps at least two of said second dice, thereby defining overlap areas, wherein said first half-capacitors located in said overlap areas are configured to be capacitively

coupled to some of said second half-capacitors,

wherein said first dice or said second dice have raised areas relative to said surfaces, the raised areas of each of said first or said second die contacting an area on one of the overlapping die.

215. (previously presented) The method of claim 214 wherein each of said first dice and said second dice have raised areas relative to said surfaces, and the signals pads in said overlapping areas are disposed in between said raised areas.

216. (previously presented) The method of claim 214 wherein each of said raised areas of said first dice contact one of the raised areas of said second dice.

217. (previously presented) The method of claim 214 wherein said plurality of first dice are on a plane that is above each of said plurality of second dice.

218. (previously presented) The method of claim 214 wherein the plurality of first dice comprises half-capacitors that do not overlap one of the plurality of second dice.

219. (previously presented) The method of claim 214

wherein arranging said first dice further comprises arranging said first dice so that each first die overlaps at least three of said second dice.

220. (previously presented) A method of fabricating an integrated circuit module, comprising:

providing a plurality of first dice, said first dice each having half-capacitors formed on a surface thereof;

providing a plurality of second dice, said second dice each having half-capacitors formed on a surface thereof;

arranging said first dice so that each first die overlaps at least four of said second dice, thereby defining overlap areas; and

aligning said first dice so that half-capacitors thereof located in said overlap areas are configured to be capacitively coupled to some half-capacitors of said second dice.

221. (previously presented) The method of claim 220 wherein said plurality of first dice are on a plane that is above each of said plurality of second dice.

222. (previously presented) The method of claim 220 wherein each of the plurality of first dice comprises four

sides, and each of said first dice overlaps one of said plurality of second dice on each of said four sides of said first dice.

223. (previously presented) The method of claim 220 wherein the plurality of first dice comprises half-capacitors that do not overlap one of the plurality of second dice.

224. (previously presented) The method of claim 220 wherein at least some of said half-capacitors in said plurality of first dice are capacitively coupled to a chip substrate within said first dice.

225. (previously presented) The method of claim 220 wherein at least some of said half-capacitors in said plurality of first dice are coupled to a chip substrate through vias within said first dice.